Docket No.: 60188-156 PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Masahiro FUKUI, et al. :

Serial No.: : Group Art Unit:

Filed: March 01, 2002 : Examiner:

For: WIRING METHOD IN LAYOUT DESIGN OF SEMICONDUCTOR INTEGRATED

CIRCUIT, SEMICONDUCTOR INTEGRATED CIRCUIT AND FUNCTIONAL

MACRO

#### PRELIMINARY AMENDMENT

Commissioner for Patents Washington, DC 20231

Sir:

Prior to examination of the above-referenced application, please amend the application as follows:

#### IN THE CLAIMS:

## Please amend the Claims as follows:

- 16. The semiconductor integrated circuit of Claim 13, wherein the width of the plurality of interconnection lines is  $0.18 \,\mu m$  or less.
- 17. The semiconductor integrated circuit of Claim 13, wherein the plurality of interconnection lines are a plurality of address bus lines.

18. The semiconductor integrated circuit of Claim 13, wherein signals propagating through the plurality of interconnection lines are digital signals of an image or voice.

Please add new claims 35-40 as follows:

- --35. The semiconductor integrated circuit of Claim 14, wherein the width of the plurality of interconnection lines is  $0.18 \,\mu m$  or less.
- 36. The semiconductor integrated circuit of Claim 15, wherein the width of the plurality of interconnection lines is  $0.18 \,\mu m$  or less.
- 37. The semiconductor integrated circuit of Claim 14, wherein the plurality of interconnection lines are a plurality of address bus lines.
- 38. The semiconductor integrated circuit of Claim 15, wherein the plurality of interconnection lines are a plurality of address bus lines.
- 39. The semiconductor integrated circuit of Claim 14, wherein signals propagating through the plurality of interconnection lines are digital signals of an image or voice.
- 40. The semiconductor integrated circuit of Claim 15, wherein signals propagating through the plurality of interconnection lines are digital signals of an image or voice.--

#### REMARKS

The above-referenced application is amended to delete the multiple dependency of claims 16-18 to avoid the multiple dependent claim filing fee. New claims 35-40 correspond to claims

16-18 rewritten so as to eliminate the mutliple dependency. Attached hereto is a marked-up version of the claims as amended. Entry of this preliminary amendment is respecfully requested.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Michael E Fogarty Registration No. 36,139

600 13<sup>th</sup> Street, N.W. Washington, DC 20005-3096 (202) 756-8000 MEF:prp **Date: March 1, 2002** 

Facsimile: (202) 756-8087

Docket No.: 60188-156

# MARKED-UP VERSION OF AMENDED CLAIMS

## The Claims have been amended as follows:

16. The semiconductor integrated circuit of Claim 13, [any of Claims 13, 14 and 15] wherein the width of the plurality of interconnection lines is  $0.18 \,\mu\text{m}$  or less.

17. The semiconductor integrated circuit of <u>Claim 13</u>, [any of Claims 13, 14 and 15] wherein the plurality of interconnection lines are a plurality of address bus lines.

18. The semiconductor integrated circuit of <u>Claim 13</u>, [any of Claims 13, 14 and 15] wherein signals propagating through the plurality of interconnection lines are digital signals of an image or voice.

The following claims have been added:

- 35. The semiconductor integrated circuit of Claim 14, wherein the width of the plurality of interconnection lines is  $0.18 \,\mu m$  or less.
- 36. The semiconductor integrated circuit of Claim 15, wherein the width of the plurality of interconnection lines is  $0.18 \,\mu m$  or less.
- 37. The semiconductor integrated circuit of Claim 14, wherein the plurality of interconnection lines are a plurality of address bus lines.
  - 38. The semiconductor integrated circuit of Claim 15, wherein the plurality of

interconnection lines are a plurality of address bus lines.

- 39. The semiconductor integrated circuit of Claim 14, wherein signals propagating through the plurality of interconnection lines are digital signals of an image or voice.
- 40. The semiconductor integrated circuit of Claim 15, wherein signals propagating through the plurality of interconnection lines are digital signals of an image or voice.